

IN THE CLAIMS:

1. (Currently Amended) A film forming method for forming a silicon-containing barrier insulating film on a substrate comprising the steps of:

(a) preparing a film-forming gas comprising, (1) at least one member selected from the group consisting of alkoxy compounds having Si-H bonds and siloxane compounds having Si-H bonds and (2) at least one oxygen-containing gas selected from the group consisting of O₂, N₂O, NO₂, CO, CO₂, and H₂O;

(b) converting the film-forming gas into a plasma;

(c) contacting the substrate with the plasma to form the silicon-containing barrier insulating film on the substrate; and

(d) forming a porous insulating film by plasma enhanced CVD or forming a SiOF film, as an interlayer insulating film, directly on said barrier insulating film ~~by coating or plasma enhanced CVD.~~

2. (Previously Amended) A film forming method according to claim 1, wherein at least one member selected from a group consisting of N₂ and H₂ is added to the film-forming gas.

3. (Previously Amended) A film forming method according to claim 1, wherein (1) is trimethoxysilane (TMS:SiH(OCH₃)₃).

4. (Previously Amended) A film forming method according to claim 1, wherein (1) is tetramethyldisiloxane ($\text{TMDSO}:(\text{CH}_3)_2\text{HSi-O-SiH}(\text{CH}_3)_2$).
5. (Previously Amended) A film forming method according to claim 1, wherein parallel-plate type electrodes are employed as a plasma generating means, and wherein high frequency power having a frequency of 100 kHz to 1 MHz is applied to an electrode on which the substrate is loaded and high frequency power having a frequency of 1 MHz or more is applied to an electrode opposing the electrode on which the substrate is loaded.
6. (Previously cancelled)
7. (Previously cancelled)
8. (Currently Amended) A semiconductor device manufacturing method according to claim 1 6, wherein said interlayer insulating film has a greater thickness than the barrier insulating layer.
9. (Withdrawn) A semiconductor device in which a silicon-containing insulation film whose peak of an absorption intensity of an infrared rays is in a range of a wave number 2270 to 2350 cm^{-1} , whose film density is in a range of 2.25 to 2.40 g/cm^3 , and whose relative dielectric constant is in a range of 3.3 to 4.3 is formed on a substrate.

10. (Withdrawn) A semiconductor device according to claim 9, further comprising a wiring is formed on a surface of the substrate,

wherein the silicon-containing insulation film covering the wiring to come into contact with the wiring.

11. (Withdrawn) A semiconductor device according to claim 9, further comprising:

a wiring;

an insulating film that covers the wiring to come into contact with the wiring are formed on a surface of the substrate; and

an protection layer made of the silicon-containing insulation film formed on the insulating film.

12. (Withdrawn) A semiconductor device according to claim 9, further comprising:

a wiring formed on a surface of the substrate; a lower protection layer that covers the wiring to come into contact with the wiring;

a main insulating film that is laminated on the lower protection layer to come into contact with the lower protection layer; and

an upper protection layer that is laminated on the main insulating film to come into contact with the main insulating film,

wherein both the lower protection layer and the upper protection layer are made of the silicon-containing insulation film.

13. (Withdrawn) A semiconductor device according to claim 12, wherein the main insulating film is made of any one selected from the group consisting of an SiOF film and a porous insulating film.

14. (Withdrawn) A semiconductor device according to claim 9, further comprising:

an lower wiring;

a upper wiring; and

an interlayer insulating film interposed between the lower wiring and the upper wiring are formed on the substrate, wherein the interlayer insulating film is made of the silicon-containing insulation film.

15. (Withdrawn) A semiconductor device according to claim 14, wherein the lower wiring and the upper wiring are connected via an opening portion formed to perforate the interlayer insulating film.

16. (Withdrawn) A semiconductor device according to claim 9, further comprising:

(I) a lower wiring formed on a surface of the substrate (20c);

(ii) an upper wiring; and

(iii) an interlayer insulating film interposed between the lower wiring and the upper wiring, the interlayer insulating film comprising

(a) a lower protection layer made of the silicon-containing insulation film that covers the lower wiring to come into contact with the lower wiring,

(b) a main insulating film that is laminated on the lower protection layer to come into contact with the lower protection layer, and

(c) an upper protection layer made of the silicon-containing insulation film that is laminated on the main insulating film to come into contact with the main insulating film,

wherein both the lower protection layer and the upper protection layer are made of the silicon-containing insulation film.

17. (Withdrawn) A semiconductor device according to claim 16, wherein the main insulating film is any one selected from a group consisting of an SiOF film and a porous insulating film.

18. (Withdrawn) A semiconductor device according to claim 16, further comprising:

an opening portion formed to perforate the interlayer insulating film; and

a side-wall protection layer made of the silicon-containing insulation film is formed on a side wall of the opening portion,

wherein the lower wiring and the upper wiring are connected via the opening portion.

19. (Currently Amended) A semiconductor device manufacturing method comprising:

forming wiring on a surface of a substrate;

preparing a film-forming gas comprising, (1) at least one member selected from the group consisting of alkoxy compounds having Si-H bonds and siloxane compounds having Si-H bonds and (2) at least one oxygen-containing gas selected from the group consisting of O₂, N₂O, NO₂, CO, CO₂, and H₂O;

converting the film-forming gas to a plasma;
contacting the surface of the substrate with the plasma to form a silicon-containing barrier insulating film directly on the wiring substrate; and
forming a porous insulating film by plasma enhanced CVD or forming a SiOF film, as an interlayer insulating film, directly on said barrier insulating film.

20. (Previously Added) A film-forming method according to claim 1 wherein (1) is TMS and (2) is N_2O and wherein the volumetric ratio of $\text{N}_2\text{O}/\text{TMS}$ is about 30:1.

21. (Currently Cancelled)

REMARKS

This amendment is in response to the "final" office action of June 18, 2003 and is herewith filed with a Request for Continued Examination (RCE).

A petition for a one month extension of time has today been filed as a separate paper and a copy is attached hereto.

The examiner will note that both of independent claims 1 and 19 have been amended to include the limitation of cancelled claim 21, modified to more correctly correspond to the teachings of applicants' specification. At page 42, lines 3-6 of their specification, applicants teach that the "porous insulating film 35" of the fifth embodiment may be formed by a PE-CVD method. Also see page 35, lines 11-14 for a teaching that the insulating film 25 in the fourth embodiment may be either a porous insulating film or a SiOF film. It is respectfully submitted that the manner in which the limitation of claim 21 has been written into claims 1 and 19 provides a clarification of the point raised by the examiner in paragraph 5 of the office action. Stated differently, it is believed that the rejection of claim 21 for indefiniteness is now moot. In view of the fact that claim 21 was not rejected over prior art, it is believed that all claims are now in condition for allowance.

The rejection of claims 1, 3, 4 and 19 for anticipation by Maeda is respectfully traversed on the basis of the present amendments. Likewise, the rejection of claim 2 for obviousness over

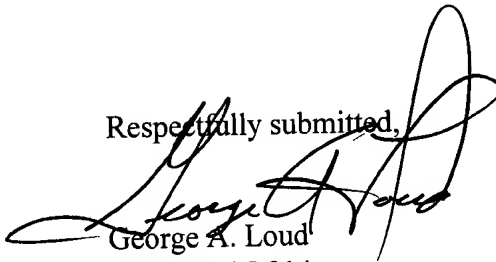
Saito et al is respectfully traversed. The references Maeda et al (U.S. 5,554,570), and Saito et al (JP 08-236518) are both directed to elimination of dependence of film formation by thermal CVD upon the nature of the surface on which the film is formed. The insulating films of the references are used as a base for the thermal CVD film formation. Further, Saito et al (JP 09-134910) forms an interlayer insulating film, not a barrier insulating film. On the other hand, the present invention forms a barrier insulating film. The barrier insulating film according to the present invention has low dielectric constant and is superior in preventing moisture from permeating an adjacent interlayer insulating film. While Maeda et al (U.S. 5,554,570) disclose an example of forming a barrier insulating film on an interlayer insulating film, the insulating film sandwiched between barrier layers is different from that of the present invention. In the present invention the insulating film in contact with the barrier layer is a porous insulating film formed by a plasma enhanced CVD or an SiOF film, while it is a SiO₂ insulating film formed by thermal CVD in Maeda et al.

Because both of the references are directed to elimination of the dependence of thermal CVD film formation on the nature of the surface on which the film is deposited by thermal CVD, it would not have been obvious to substitute applicants' step d for the thermal CVD of the references. More specifically, both Maeda et al and Saito et al employ the respectively disclosed plasma enhanced CVD for film formation to provide a more suitable surface for subsequent formation of an SiO₂ film thereon by thermal CVD. Accordingly, substitution of applicants' step d for the thermal CVD step of Maeda et al or Saito et al eliminates the rationale of these references for employing the plasma assisted CVD film as an underlying layer.

Claim 8 has been amended to depend upon claim 1 to obviate the basis for its rejection for indefiniteness in paragraph 5 of the office action.

In conclusion, it is respectfully submitted that the captioned application is now in condition for allowance.

Respectfully submitted,



George A. Loud
Reg. No. 25,814

Dated: October 16, 2003

LORUSSO, LOUD & KELLY
3137 Mount Vernon Avenue
Alexandria, VA 22305

(703) 739-9393